CPRE 4910 Weekly Report 09

11/18/2025 - 12/2/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

  This week we presented our improved diagram showing how data will flow. There was a heavy emphasis on memory, caching, and core implementation.

- **Past Week Accomplishments**
  - Colin McGann: Finished testing on the pipelined divider
  - Jack Tonn: Catching design document caught up to current design, refining ISA. Finished core design based on ISA and put it in the design doc.
  - Dawud Benedict: Thinking through HDL implementation of vertex cache. Looking at commercial SRAM cache with DFF metadata.
  - Michael Drobot: Wrote div and mod procedures, created procedure call convention, wrote design doc ISA section, updated ISA definitions
  - Sam Forde: Design document, wrote a divider testbench in SVUnit, imported commercial SRAM into design.
  - Josh Arceo: Started cache section of design doc
  - Emil Kosic: Began Verilog of shift unit, worked on presentation slides

- **Pending Issues**
    - Core design, Design doc and Faculty Presentation
- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Colin McGann	Finished the divider pipeline	10	130
Jack Tonn	ISA design, core design, design doc	35	91
Dawud Benedict	Rethinking memory hierarchy	10	66
Michael Drobot	ISA procedures and definitions, design doc ISA section	32	152
Sam Forde	Design document, divider, implement sram	8	59
Josh Arceo	Cache Design Doc	5	40
Emil Kosic	Presentation work and shift unit	5	42

- **Plans for the upcoming week**
    - Colin McGann: Will work on the design doc and the faculty presentation.
    - Jack Tonn: Faculty presentation prep and design doc. Core controller design
    - Dawud Benedict: Presentation. Finalize memory and cache in design document.
    - Michael Drobot: Finish updating core controller, test all existing shader programs. Keep working on the core controller.
    - Sam Forde: Work on design doc and final presentation.
    - Josh Arceo: Work on design doc.
    - Emil Kosic: Work on wrapping up design work and design units on the side